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Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have not been amended.

No new matter has been added.

Applicants respectfully request reconsideration of Applicants claims.

Claim Rejections under 35 USC 103(a)

1. Claims 1, 3-5, 7-8, 11-12, 15-17, 19, 21, and 22 stand rejected under 35 USC 103(a) as being unpatentable over Ishii et al., (US 5,571,366) in view of Somekh et al. (US 5,643,366) or Brors et al. (EP 0276061).

Ishii et al. disclose a plasma processing apparatus whereby the plasma pressure or light emitted from the plasma is monitored

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in-situ and a voltage source for supplying a radiofrequency is controlled in response to the in-situ monitoring (see abstract).

Ishii et al. disclose a vertically moveable wafer support (wafer lifter) mechanism (see col 11, line 32-36; Figure 12, item 76) is disclosed to support a wafer held by an electrostatic chuck (item 12) in a face down position together with a vertically moveable pusher pin mechanism (item 77) embedded in the electrostatic wafer chuck to remove the wafer from the electrostatic chuck following wafer processing. Ishii et al. does not disclose the structure of the vertically moveable support mechanism (item 76) other than what is shown in Figure 12. Figure 12 shows the wafer support (item 76) having a left and right fingers (arms) that support the **wafer processing surface from below** on the periphery (item W). Ishii et al. disclose that in the face down position, the wafer process surface can be protected from being contaminated by fine particles (col 11, lines 37-40). The wafer lifter structure of Ishii et al. extends into the plasma processing volume would likely interfere with a plasma process.

Thus, the wafer support structure of Ishii et al. holds the wafer **in an upside down position with an electrostatic wafer chuck** and is further **supported from below by a two fingered wafer lifter touching the wafer periphery**.

Thus, Ishii et al. does not disclose several aspects of the claimed structure and operation of Applicants claimed semiconductor wafer lifter including:

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"a vertically moveable wafer lifter to hold a semiconductor wafer in a face down processing position during plasma processing at a top of the plasma chamber, the semiconductor wafer and the wafer lifter supplied with an electrical bias during plasma processing;

wherein the wafer lifter further comprises sidewalls defining a first diameter greater than a diameter of the semiconductor wafer and a bottom portion having a circular opening therein, said circular opening having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer; and,

wherein the semiconductor wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose only the semiconductor wafer processing surface face down during plasma processing."

The two fingered support of Ishii et al., extends through a plasma volume below the processing surface to support the wafer processing surface from below and therefore would likely interfere a plasma process, defeating an advantage of Applicants disclosed and claimed invention.

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Ishii et al. further does not disclose or suggest that an electrical bias is or can be supplied through a semiconductor wafer lifter. Rather in the apparatus of Ishii et al. the semiconductor wafer holder is taught only to be electrically biased **through the electrostatic chuck.**

Ishii et al. fail to disclose several aspects of Applicants disclosed and claimed wafer lifter structure. Moreover, and the wafer lifter of Ishii et al. operates by a different principal of operation than the claimed structure of Applicants, i.e., Ishii et al. disclose a **two fingered wafer lifter structure touching the semiconductor process face only at two points on the wafer periphery, while exposing side portions of the wafer, and extending through a plasma processing volume.** Moreover, even assuming arguendo that Ishii et al. disclose biasing the two fingered (armed) wafer support, the **two fingered wafer lifter is structurally different** from Applicants disclosed and claimed invention.

Examiner argues that "as shown in Figure 12, the wafer lifter contacts portions of the apparatus that are applied with electrical bias and therefore, inherently, the wafer lifter will be supplied with an electrical bias."

Applicants respectfully point out that the wafer lifter of Ishii et al. is shown to contact only peripheral portions of the wafer process surface, **which may be electrically insulated from the electrostatic chuck by an insulating layer commonly present on a processing surface of a semiconductor processing wafer.** There is no teaching or suggestion in Ishii et al., that the

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wafer lifter is supplied with an electrical bias. Applicants respectfully reject any assertion of inherency by Examiner.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich*, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).

For example, Somekh et al., discloses a "C" shaped wafer support (wafer lifter) with a **three fingered contact surface** to raise a semiconductor wafer to contact a susceptor (wafer chuck) (see abstract, col 2, lines 6-18;). The wafer lifter (wafer support assembly) is **then lowered and moved out of the path of the susceptor (i.e., chuck)** (col 2, lines 26-30) which is then lowered for plasma processing. The purpose of the "C" shaped wafer support is to allow the **susceptor arm to move the susceptor holding the wafer downward** into a plasma processing position **after the wafer support is removed from the wafer** (col 3, lines 1-8).

Thus, the apparatus of Somekh et al. works by a **different principle of operation** than the apparatus of Ishii et al.

Examiner argues that the fact that the wafer support of Somekh et al. **moves out of the way during processing** merely recites intended use. Applicants respectfully point out that the argument made is that there is no motivation for combining the structures of Ishii et al. and Somekh et al., since they work by

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a different principle of operation. Even assuming *arguendo*, a proper motivation for combination, any conceivable modification of either reference, which Examiner has not pointed out, would not produce Applicants structure or achieve Applicants claimed operation and would make the structures of both Ishii et al. and Somekh et al. **unsuitable for their intended purpose**. Examiner cites no support for the assertion that a successful plasma process could take place with the wafer lifter of Somekh et al. in place, and nevertheless, such a configuration **defeat an advantage of Applicants invention**, where the wafer support **need not be moved during plasma processing**, and would likely interfere with the varying magnetic fields and plasma process in the reactor of Applicants.

On the other hand, Brors et al. disclose a plasma chamber for CVD deposition including a **manipulator arm and blade (wafer lifter)** that **transfers a wafer from a cassette in a loading chamber** to underneath a wafer chuck located at a top portion of the plasma chamber by rotating horizontally 90 degrees. A **3-arm lifting mechanism** on the blade, each arm having ceramic fingers then lifts the wafer to contact the chuck, similar to Somekh et al.:

"The manipulator arm 68 is rotated by a motor through a 90 DEG angle. The loadlock 64 is opened and the manipulator arm 68 extends carrying the blade 70 with wafer 46 into the center of the deposition chamber 16. **Three lifting arms 72 each having a ceramic finger 74 approximately one-eighth inch in diameter attached to support 71, lift the wafer 46 off the blade and contact the back side of the wafer 46, face down, with the chuck 76.** A larger number of

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ceramic fingers can be used to avoid the necessity of prealigning the wafer to orient the flat, however, typically 3 fingers are used with prealignment of the wafers in the cassette."

Examiner argues that Applicants structure is shown in Figure 14 of Brors et al. Applicants respectfully suggest Examiner is mistaken and here reproduce the only description relating to Figure 14 and the disclosed structure which **does not disclose or suggest a wafer lifter, but discloses a wafer clamp assembly:**

FIG. 14. A vacuum-tight reaction chamber 210 formed of metal or similar material is fitted with a cooling channel 212 and other cooling channels (not shown). A gas mix chamber 214 is attached below the reaction chamber 210. Gas mix chamber 14 is equipped with suitable cooling channels (not shown). Gas injector rings 216, 218 are connected through suitable feedthroughs in the bottom plate of the gas mix chamber 214 to sources of process gas external to the apparatus. A ring insulator 216 is used between the reaction chamber 210 and the mix chamber 214 to facilitate independent temperature control. A water cooled chuck holder 222 is located at the top of the reaction chamber. The interior faces 224 of the chuck holder 222 can be polished and sloped as shown or vertical with a step at the bottom. The upper surface of the chuck holder 222 is sealed to a quartz window 226 to provide a vacuum wall which passes radiant energy. The size of the quartz window is determined by the size of the radiant energy source 228; the larger the energy source the larger the quartz window 226 must be, allowing larger wafers to be coated. **At the bottom of the chuck holder 222 there is a ring chuck 230 of quartz or other suitable material the interior diameter of which is slightly smaller than the wafer to be processed. The wafer 232 is held face down to the ring 230 with a wafer clamp assembly 234.** An insulating ring 236 is provided to electrically insulate the chuck 222 from the reaction chamber 210. The top of the reaction chamber 210 is fitted with a plurality of exhaust ports 238. The gas mix chamber 214 is connected to the reaction chamber 210 so as to direct a flow of mixed reaction gases at the wafer 232. A gas duct 240 is used to guide the flow of gases to the wafer. A gas deflector 242 is centered in the opening between the reaction chamber 210 and mix chamber 214. The gas deflector 242 is mounted

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on a shaft 244 which passes through a gland 246 facilitating a slidable seal so that the gas deflector 242 may be adjusted in vertical position within the opening to deflect the gas to get a uniform deposition on the substrate. Shaft 246 is made hollow and there is a hole in the center of gas deflector 242 so that pyrometer 248 can be sealed to shaft 244 outside the vacuum. Pyrometer 248 is aimed at the wafer 232 to measure its temperature and provide feedback for temperature control.

Thus, the structure of the wafer support (lifter) of Somekh et al. or Brors et al. (or a clamp assembly) are different from, and work by a different principle of operation, than **both** the apparatus of Ishii et al. and Applicants disclosed and claimed invention. The wafer lifter of Somekh et al. or Brors et al. **does not hold the wafer at a top of the plasma chamber during plasma processing**, but rather raises the wafer to contact a susceptor (wafer chuck), which holds the wafer during processing while the wafer lifter is **moved out of the way of the plasma process**. The **three-fingered wafer lifter structure** of Brors et al. or Somekh et al., or the **wafer clamp assembly** of Brors et al., does not disclose Applicants wafer lifter structure. The **two-fingered wafer lifter of Ishii et al.** does not disclose Applicants wafer lifter structure and moreover, is held in place **below the wafer during plasma processing, which would interfere with Applicants plasma process**. Any combination of the above references does not produce Applicants wafer lifter structure or Applicants dry etching system.

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Thus even assuming *arguendo*, some motivation other than Applicants disclosure for combining the references, the combination of the **two-fingered** wafer lifter of Ishii et al. and the **three-fingered** wafer lifters of Somekh et al. or Brors et al. (or the wafer clamp assembly), does not produce Applicants disclosed and claimed wafer lifter structure or Applicants dry etching system.

Moreover, the **two fingered structure** of Ishii et al. and the **three fingered structures** of Somekh et al. or Brors et al. (or the wafer clamp assembly of Brors et al.), do not produce Applicants claimed structure and could not accomplish the principal of operation of Applicants structure, including **supplying a bias to the wafer lifter during plasma processing as claimed and disclosed by Applicants**;

Or

"wherein the wafer lifter further comprises **sidewalls** defining a first diameter greater than a diameter of the semiconductor wafer and a **bottom portion having a circular opening therein**, said circular opening having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer; and,

wherinc the semiconductor **wafer periphery rests on an inner top surface of the bottom portion** defining the circular opening

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to expose only the semiconductor wafer processing surface face down during plasma processing".

The combined teachings of Ishii et al., Somekh et al. and/or Brors et al. are clearly insufficient to make out a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention since they do not show or suggest Applicants wafer lifter structure or Applicants dry etching system.

"Finally, the prior art reference (or references when combined) must **teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaccek*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Examiner argues that **regardless of the differences in the structure** of Applicants disclosed and claimed invention and the combined teachings of Ishii et al. and Somekh et al. or Brors et al., that "**a prima facie case of obviousness still exists because no unexpected results have been shown**". Applicants respectfully suggest Examiner is mistaken in suggesting that a *prima facie* case can be made out without showing Applicants claimed invention or suggestion thereof in the prior art.

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Applicants respectfully point out that Examiner, in impermissibly attempting to shift the burden of establishing a *prima facie* case of non-obviousness to Applicants, argues that "there is no evidence that **exposing only the semiconductor processing surface face down would significantly affect the overall performance of the plasma processing**". Applicants respectfully suggest that Examiner is mischaracterizing Applicants **invention taken as a whole**, and is ignoring the teachings in Applicants specification, as well as the teachings in the cited art including that of Somekh et al. or Brors et al. who teach **moving the wafer lifter out of the way** during plasma processing. Nevertheless, the cited references do not disclose Applicants wafer lifter structure or Applicants dry etching system and Applicants respectfully point out that the burden remains on Examiner to show Applicants claimed invention in the prior art, which Examiner has not shown.

Examiner argues that the fact that Somekh et al. or Brors et al. do not show the wafer lifter holding the wafer in place **during plasma processing**, is merely a recitation of intended use. Examiner ignores the fact that the combined references **do not show Applicants claimed wafer lifter structure or Applicants dry etching system**. **All the cited references disclose etching or deposition systems have wafer lifters with fingered supports**.

It is clear that the combined references do not show or suggest Applicants structure:

"whereto the wafer lifter further comprises sidewalls

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defining a first diameter greater than a diameter of the semiconductor wafer and a bottom portion having a circular opening therein, said circular opening having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer; and,

wherein the semiconductor wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose only the semiconductor wafer processing surface face down during plasma processing."

Therefore Examiner has failed to make out a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention.

2. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Ishii et al., (US 5,571,366) in view of Somekh et al. (US 5,643,366) or Brors et al. (EP 0276061), as applied above, and further in view of Uchida (US 5,804,027) or Ishii et al. (US 5,795,429).

Applicants reiterate the comments made above with respect to Ishii et al., Somekh et al. or Brors et al.

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In addition, even assuming *arguendo*, proper motivation for combination, the combination of the teachings of Ishii et al., with Somekh et al. or Brors et al., and further in view of Uchida or Ishii et al. '429, the fact that Uchida or Ishii '429 show an apparatus with electromagnetic coils to generate electromagnetic fields does not produce Applicants disclosed and claimed invention and does not further help Examiner in making out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

3. Claims 10 and 18 stand rejected under 35 USC 103(a) as being unpatentable over Ishii et al., (US 5,571,366) in view of Somekh et al. (US 5, 643, 366) or Brors et al. EP 0276061, as applied above, and further in view of Admitted Prior Art.

Applicants reiterate the comments made above with respect to Ishii et al., Somekh et al. or Brors et al.

Applicants further respectfully point out that Examiner is erroneously looking to Applicants disclosure **for a suggestion to combine the teachings of references**, i.e., as a roadmap to

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recreate Applicants disclosed and claimed invention, which Applicants respectfully point out is impermissible.

Nevertheless, in Applicants discussion of the prior art, Applicants merely disclose problems with a plasma processing chamber where a wafer is held in a face-up position during plasma processing. Thus, even assuming *arguendo*, proper motivation for combination, the combination of Ishii et al. with Somekh et al. or Brors et al., and further in view of Applicants alleged admitted prior art, does not produce Applicants disclosed and claimed invention and does not further help Examiner in making out a *prima facie* case of obviousness.

"The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not based on applicant's disclosure.**" *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

4. Claims 1, 3, 5, 7-8, 10-12, and 15-19 stand rejected under 35 USC 103(a) as being unpatentable over Admitted Prior Art in view of Ishii et al., (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Brors et al. (EP 0276061).

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Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Ishii et al., and Somekh et al. or Brors et al.

As pointed out above, even assuming *arguendo*, proper motivation for combination of the above references, such combination does not produce Applicants disclosed and claimed invention and does not further help Examiner in making out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaccek*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

5. Claim 9 stands rejected under 35 USC 103(a) as being unpatentable over Admitted prior art in view of Ishii et al. (US 5,571,366), and Somekh et al. (US 5, 643, 366) or Brors et al. EP 0276061, as applied above, and further in view of Uchida (US 5,804,027) or Tshii et al. (US 5,795,429).

Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art, Tshii et al., and Somekh et al. or Brors et al.

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As pointed out above, even assuming *arguendo*, proper motivation for combination, the combination of Applicants alleged admitted prior with and Ishii et al., and Somekh et al. or Brors et al., and further in view of Uchida or Ishii et al. '429, does not produce Applicants disclosed and claimed invention and does not help Examiner in making out a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Conclusion

Applicants respectfully request reconsideration of their claims and submit that the claims are in condition for allowance.

Such favorable action by the Examiner at an early date is respectfully solicited.

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In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040